## REMARKS

Claims 1-17 are pending in the application prior to entering this amendment.

The examiner rejects claims 1, 3-6 and 11-17 under 35 U.S.C. § 103(a) as being unpatentable over Cappels, Sr. (U.S. Patent No. 5,731,843) in view of Levantovsky et al. (U.S. Patent No. 6,522,365). The examiner rejects claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Cappels in view of Levantovsky and further in view of Koike et al. (U.S. Patent No. 6,538,648). The examiner rejects claims 7-10 under 35 U.S.C. § 103(a) as being unpatentable over Cappels in view of Levantovsky and further in view of Ichiraku (U.S. Patent No. 6,097,379).

The applicants amend claim 1 and cancel claim 4 without prejudice.

Claims 1-17 remain in the application after entering this amendment.

The applicants add no new matter and request reconsideration.

### Claim Rejections Under § 103

The examiner rejects claims 1-17 as old over various combinations of Cappels, Levantovsky, Koike, and Ichiraku. The applicants disagree for the reasons that follow.

The present application describes and claims an improved automatic phase and frequency adjust circuit and method. The automatic phase and frequency adjust circuit addresses the need to make fast and accurate adjustments to a pixel clock used to digitize analog image data. The automatic phase and frequency adjust circuit accomplishes these improvements due in part to the operation of the phase adjust circuit 245 (Figure 2) that generates a pixel clock 228 responsive to a phase signal 238 and the phase detector circuit 247 that operates responsive to the clock phases 260 and the phase signal 238.

Cappels, on the other hand, discloses in its abstract an apparatus and method for automatically adjusting a pixel sampling clock frequency and phase of a *video display* to match the frequency and phase of a *pixel clock* used to generate an incoming video signal. Cappels does not disclose an apparatus to adjust the pixel clock itself.

Claim 1 recites *an edge detector circuit to generate an edge pulse signal... responsive to a pixel clock.* The examiner alleges Cappels discloses the recited edge detector as "the differentiator 52 [sic] and the threshold detector 44." And the examiner alleges Cappels discloses that the "differentiator 42 and the threshold detector 44 function together to detect voltage transitions between pixel instructions, also called pixel edges." Cappels, Figure 3, and column 4, lines 41-44. The examiner goes one to identify the phase adjust circuit to generate a

pixel clock as the phase adjuster 50 which produces an adjusted pixel sampling clock 64 that matches the phase of the video signal 52. Cappels, Figures 3 and 4, and column 5, line 15 to column 6, line 31. If Cappels' differentiator 42 and threshold detector 44 disclose the recited edge detector and the pixel sampling clock 64 discloses the recited pixel clock, as the examiner alleges, the differentiator 42 and threshold detector 44 must operate responsive to the clock 64 if Cappels is to obviate the claim. They do not.

And claim 1 recites *a phase detector circuit to generate a phase adjust signal responsive to a phase of the phase locked loop clock and the edge pulse signal.* The examiner alleges the phase detector circuit is disclosed by the comparator 46 and the microprocessor 48. And the examiner identifies the pixel clock 55 as generating the recited phase locked loop circuit that generates the phase locked loop clock. But if the output of pixel clock 55 discloses the phase locked loop clock, then the comparator 46 and the microprocessor 48 must operate responsive to that output if it is to meet the claims. As is clearly seen in Figure 3, Cappels does not operate as recited. Put differently, and as shown in Figure 3, neither Cappels' microprocessor 48 nor the comparator 46 operate responsive to (or receive input from) the pixel clock 55, as they must to disclose claim 1. Further, the combination of the comparator 46 and the microprocessor 48 do not operate to generate a phase adjust signal responsive to a phase of the phase locked loop clock (alleged to be the output of the pixel clock 55) and the edge pulse signal (acknowledged by the examiner as not disclosed by Cappels at all).

And claim 1 recites *an edge detector circuit to generate an edge pulse signal corresponding to a transition of an analog data signal above a predetermined threshold responsive to a pixel clock.* The examiner acknowledges that Cappels does not disclose the recited edge detector that operates responsive to a pixel clock but argues Levantovsky provides the missing link. The examiner alleges Levantovsky's edge detection module 64 discloses the recited edge detector circuit. If so, the module 64 generates the recited edge pulse signal. A person of reasonable skill in the art would therefore be required to provide Levantovsky's module 64 into Chapels' system to solve a problem for which Cappels provides its own complete solution. And a person of reasonable skill in the art would have to necessarily have to know to provide the output of Levantovsky's module 64 into the input of Cappels' comparator 46 and the microprocessor 48 to meet the recited limitations. The combination, therefore, requires excessive experimentation without due motivation.

Even if a person of reasonable skill in the art where inclined to modify Cappels by adding Levantovsky's module 64 to disclose the recited claims, the combination would not produce an

operable system. This is because Levantovsky's module 64 "has an input 76 coupled to the output 74 of the ADC 62 and an output 78 to provide the pixel coordinates of the earliest on-transition and latest off-transition times for each video frame." Column 6, lines 60-63. In contrast, the recited edge detector generates an edge pulse signal (of arbitrary width) *corresponding to a transition of the analog signal above a predetermined threshold.* No such threshold is disclosed in Cappels or Levantovsky.

In considering claim 4, the examiner alleges that Cappels' "differentiator 95 [sic] and the threshold detector 100 [sic] which is function together to produce the pulse signal." But the examiner has previously identified the comparator 46 and the microprocessor 48 as disclosing the recited edge detector, so they (46 and 48) must operate to generate the recited pulse signal when the analog signal is above a predetermined threshold. Neither the comparator 46 nor the microprocessor 46 generates the signal 56 as they must to meet the recited limitations. It appears to the applicants that the examiner is attempting to cobble together pieces of references to obviate the claims. To do so effectively, however, the pieces must be connected and operate as the claims require. Since the pieces are not so connected and do not so operate, claims 1-17 are in condition for allowance.

**Conclusion**

The applicants request reconsideration and expeditious issuance of all remaining claims. The applicants encourage the examiner to call the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on February 28, 2006.

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Respectfully submitted,

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